CLAIM LISTING

Please amend the claims as shown below:

1. (Currently Amended) A method of processing digital communication signals in a system including a receiver, a processor and a plurality of buffers, the method comprising:

buffering first digital samples received from the receiver and corresponding to a first group of symbols into a first buffer and a second buffer at a sample rate, wherein buffered first digital samples corresponding to earlier paths of the first group of symbols are stored in the first buffer, and buffered first digital samples corresponding to later paths of the first group of symbols are stored in the second buffer;

processing, by the processor, the first digital samples in the first buffer and the second buffer for all known paths of the first group of symbols during a first symbol group duration, wherein the processor is clocked by a processor clock at a clock rate that is faster than and not synchronous with the sample rate;

disabling the processor upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration;

simultaneously with processing the first digital samples, buffering second digital samples corresponding to a second group of symbols into the second buffer and a third buffer, wherein buffered second digital samples corresponding to earlier paths of the second group of symbols are stored in the second buffer, and buffered second digital samples corresponding to later paths of the second group of symbols are stored in the third buffer, and wherein the first symbol group duration represents a duration of time during which the second digital samples are buffered into the second buffer and the third buffer, and wherein buffering the second digital samples from the receiver is capable of occurring while the processor is disabled during the remainder of the first symbol group duration;

after completion of buffering the second digital samples and at a beginning of a second symbol group duration that occurs consecutively with an end of the first symbol group duration, enabling the processor to process the second digital samples;

processing, by the processor, the second digital samples in the second buffer and the third buffer for all known paths of the second group of symbols during the second symbol group duration;

disabling the processor upon completion of processing the second digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the second symbol group duration;

simultaneously with processing the second digital samples, buffering third digital samples received from the receiver and corresponding to a third group of symbols into the third buffer and the first buffer, wherein buffered third digital samples corresponding to earlier paths of the third group of symbols are stored in the third buffer, and buffered third digital samples corresponding to later paths of the third group of symbols are stored in the first buffer, and wherein the second symbol group duration represents a duration of time during which the third digital samples are buffered into the third buffer and the first buffer, and wherein buffering the third digital samples from the receiver is capable of occurring while the processor is disabled during the remainder of the second symbol group duration;

after completion of buffering the third digital samples and at a beginning of a third symbol group duration that occurs consecutively with an end of the second symbol group duration, enabling the processor to process the third digital samples;

processing the third digital samples in the third buffer and the first buffer for all known paths of the third group of symbols during the third symbol group duration; and

disabling the processor upon completion of processing the third digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the third symbol group duration.

2. (Original) The method of claim 1, wherein the plurality of buffers hold a number of digital samples, the number being adjusted for communication conditions.

3. (Previously Presented) The method of claim 2, wherein the communication conditions include a communication technology and anticipated maximum useful multi-path delay in an environment.

4. (Original) The method of claim 1, wherein received information relevant to a given group of transmitted symbols is processed in one iteration, without a need to store intermediate results for the given group of transmitted symbols.

5. (Cancelled)

6. (Original) The method of claim 1, further comprising tuning a receiver to a first channel, storing received symbols from the first channel, and tuning the receiver to a second channel.

7. (Previously Presented) The method of claim 6, further comprising processing symbols received from the first channel during extra cycles of processing while the receiver is tuned to the second channel.

8. (Cancelled)

9. (Currently Amended) A method of processing digital communication signals in a system including a receiver, a processor, and a plurality of buffers, the method comprising:

processing, by [[a]] the processor during a first symbol group duration, symbols corresponding to a first group of symbols to be processed and from all known paths, wherein the first group of symbols in a first path start in a first buffer and end in a second buffer;

receiving samples from the receiver at a third buffer simultaneously with processing the first group of symbols;

disabling the processor upon completion of processing the symbols corresponding to the first group by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration, wherein the first symbol group duration ends when samples in the third buffer are ready for processing, and wherein receiving the samples at the third buffer is capable of occurring while the processor is disabled;

processing, by the processor during a second symbol group duration, symbols corresponding to a second group of symbols to be processed and from all known paths, wherein the second group of symbols in a second path start in the second buffer and end in the third buffer;

receiving samples from the receiver at the first buffer simultaneously with processing the second group of symbols;

disabling the processor upon completion of processing the symbols corresponding to the second group by gating off the processor clock, wherein the processor remains disabled through a remainder of the second symbol group duration, wherein the second symbol group duration ends when samples in the first buffer are ready for processing, and wherein receiving the samples at the first buffer is capable of occurring while the processor is disabled;

processing, by the processor during a third symbol group duration, symbols corresponding to a third group of symbols to be processed and from all known paths, wherein the third group of symbols in a third path start in the third buffer and end in the first buffer, and receiving samples at the second buffer while the third group of symbols is being processed;

receiving samples at the receiver at the second buffer simultaneously with processing the third group of symbols;

disabling the processor upon completion of processing the symbols corresponding to the third group by gating off the processor clock, wherein the processor remains disabled through a remainder of the third symbol group duration, wherein the third symbol group duration ends when samples in the second buffer are ready for processing, and wherein receiving the samples at the second buffer is capable of occurring while the processor is disabled; and

adapting duration time of the processing of the first, second, and third groups based on channel and signal conditions.

10. (Currently Amended) An apparatus to process digital communication signals, the apparatus comprising:

a plurality of buffers coupled to a receiver and configured to store digital samples received from the receiver and corresponding to groups of symbols;

a processing unit coupled to the plurality of buffers; and

programmed memory having instructions directing the processing unit to process first digital samples corresponding to a first group of symbols to be processed in a plurality of buffers, the first digital samples starting in a first buffer of the plurality of buffers and ending in a second buffer of the plurality of buffers;

wherein the processing unit processes the first digital samples during a first symbol group duration, and wherein additional digital samples are received at a third buffer of the plurality of buffers simultaneously with the first digital samples being processed, and wherein the first symbol group duration represents a duration of time that ends upon completion of synchronously filling the third buffer with the additional digital samples, and

wherein, prior to an end of the first symbol group duration, the processing unit is disabled upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration, and wherein the buffers are capable of receiving the digital samples from the receiver while the processor is disabled.

11. (Previously Presented) The apparatus of claim 10, further comprising input and output busses operable to permit random access to the plurality of buffers during processing.

12. (Original) The apparatus of claim 10, wherein symbols are processed in a different group of buffers after a process iteration is complete.

13. (Currently Amended) A method of processing digital communication signals, the method comprising:

receiving a communication signal at a receiver;

communicating digital samples from the received communication signal into a first group of sample buffers, wherein the digital samples include first symbols, and wherein the first group of sample buffers receive and store the digital samples communicated by the receiver;

processing, by a processor during a first symbol group duration, the first symbols in the first group of sample buffers while simultaneously communicating, receiving, and storing additional digital samples from the receiver into a second group of sample buffers during the processing, wherein the additional digital samples include second symbols, and wherein the first symbol group duration represents a duration of time during which the second group of sample buffers is filled with the additional digital samples;

prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first symbols in the first group of sample buffers by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration, and wherein communicating, receiving, and storing the additional digital samples into the second group of sample buffers continues to occur while the processor is disabled; and

after completion of communicating, receiving, and storing the additional digital samples in the second group of sample buffers and at a beginning of a second symbol group duration, enabling the processor to process the second symbols in the second group of sample buffers during the second symbol group duration, wherein the beginning of the second symbol group duration occurs consecutively with the end of the first symbol group duration.

14. (Original) The method of claim 13, further comprising, after symbols in a symbol path are completely processed, designating sample buffers in the first group of sample buffers as being in the second group of sample buffers; and designating sample buffers in the second group of sample buffers as being in the first group of sample buffers, whereby sample buffers are rotated between processing iterations and digital sample receiving operations.

15. (Original) The method of claim 14, wherein sample buffers in the first group of sample buffers designated as being in the second group of sample buffers include all the sample buffers in the first group of sample buffers except a sample buffer having an end of a symbol path.

16. (Cancelled)

17. (Currently Amended) A method of processing digital communication signals in a system including a receiver, a processor and a plurality of buffers, the method comprising:

processing, by the processor during a first symbol group duration, first samples corresponding to a first group of symbols to be processed, wherein the first samples start in a first buffer and end in a second buffer, and simultaneously receiving second samples from the receiver at a third buffer during the processing of the first group of symbols, wherein the second samples correspond to a second group of symbols to be processed, and the first symbol group duration represents a duration of time that ends upon completion of synchronously filling the third buffer with the second samples;

prior to an end of the first symbol group duration, disabling the processor upon completion of processing the first samples corresponding to the first group by gating off the processor clock, wherein the processor remains disabled during a remainder of the first symbol group duration, and wherein receiving the second samples continues to occur while the processor is disabled;

processing, by the processor during a second symbol group duration, the second samples corresponding to the second group of symbols to be processed, wherein the second samples start in the second buffer and end in the third buffer, and simultaneously receiving third samples at the first buffer during the processing of the [[the]] second group of symbols, wherein the third samples correspond to a third group of symbols to be processed, and the second symbol group duration represents a duration of time that ends upon completion of synchronously filling the first buffer with the third samples;

prior to an end of the second symbol group duration, disabling the processor upon completion of processing the symbols corresponding to the second group by gating off the processor clock, wherein the processor remains disabled during a remainder of the second symbol group duration, and wherein receiving the third samples continues to occur while the processor is disabled;

processing, by the processor during a third symbol group duration, the third samples corresponding to the third group of symbols to be processed, wherein the third samples start in the third buffer and end in the first buffer, and simultaneously receiving fourth samples at the second buffer while during the processing of the [[the]] third group of symbols, wherein the fourth samples correspond to a fourth group of symbols to be processed, and the third

symbol group duration represents a duration of time that ends upon completion of synchronously filling the second buffer with the fourth samples; and

prior to an end of the third symbol group duration, disabling the processor upon completion of processing the symbols corresponding to the third group by gating off the processor clock, wherein the processor remains disabled during a remainder of the third symbol group duration, and wherein receiving the fourth samples continues to occur while the processor is disabled.

18. (Cancelled)

19. (Cancelled)

20. (Cancelled)

21. (Cancelled)

22. (Currently Amended) An apparatus to process digital communication signals, the apparatus comprising:

a plurality of buffers coupled to a receiver and configured to store digital samples received from the receiver and corresponding to groups of symbols;

a processing unit coupled to the plurality of buffers; and

programmed memory having instructions directing the processing unit to process first digital samples corresponding to a group of symbols to be processed in a plurality of buffers, the first digital samples starting in a first buffer of the plurality of buffers and ending in a second buffer of the plurality of buffers;

wherein the processing unit processes the first digital samples during a first symbol group duration, and wherein additional digital samples are received from the receiver at a third buffer of the plurality of buffers simultaneously with the first digital samples being processed, and wherein the processing unit is operable to select digital samples or an intermediate result from a buffer coupled to the processing unit, and

wherein, prior to an end of the first symbol group duration, the processing unit is disabled upon completion of processing the first digital samples by gating off the processor clock, wherein the processor remains disabled through a remainder of the first symbol group duration, wherein receiving the additional digital samples from the receiver at the third buffer is capable of occurring while the processor is disabled, and wherein the processor is enabled after all of the additional digital samples are received at the third buffer and simultaneously with [[at]] a beginning of a second symbol group duration, wherein the end of the first symbol group duration coincides with the beginning of the second symbol group duration.